Amendments to the Specification

Please replace the title with the following amended title:

METHODS FOR MASKLESS LITHOGRAPHY ~~DEVICE FOR SEMICONDUCTOR CIRCUIT PATTERN GENERATION~~

Please add the following new paragraph on page 1 as the first sentence of the specification directly following the title:

Cross Reference to Related Applications

This application is a continuation of copending, commonly assigned United States Patent Application No. 08/483,731, filed June 7, 1995, which is a continuation of United States Patent Application No. 08/315,905, filed September 30, 1994, now U.S. Patent No. 5,869,354, which is a division of United State Patent Application No. 07/865,412, filed April 8, 1992, now U.S. Patent No. 5,354,695, all of which are incorporated by reference herein in their entireties.

Please replace the paragraph that begins at page 7, line 20 and ends at page 9, line 9 (immediately following the heading "BRIEF DESCRIPTION OF THE FIGURES") with the following amended version of that paragraph:

Figures 1a to 1j show a dielectric and semiconductor membrane substrate in cross-section.

Figure 2 shows an etched silicon substrate membrane in cross-section.

Figures 3a, 3b show dielectric membranes with semiconductor devices.

Figure 4 shows an alignment mark of a circuit membrane in cross-section.

Figure 5 shows support structures for a membrane structure isolation structure.

Figure 6a to 6i show a circuit membrane Air Tunnel structure.

Figure 7 shows stacked circuit membranes with optical input/output.

Figure 8 shows a three dimensional circuit membrane.

Figures 9a to 9j show fabrication of a MOSFET in a membrane.

Figures 10a to 10d show fabrication of a transistor by lateral epitaxial growth on a membrane.

Figures 11a to 11f show vertical MOSFET and bipolar transistors formed on a membrane.

Figure 12a to 12g show transistor fabrication on a membrane using confined laterally doped epitaxy.

Figures 12h to 12j show cross-sections of selective epitaxial growth on a membrane.

Figures 13a to 13d show cross-sections of multi-chip modules.

Figure 14 shows a cross-section of a membrane formed on a reusable substrate.

Figure 15 shows a cross-section of the membrane of Figure 14 with a support frame attached.

Figures 16a, 16b show multi-chip nodules in packages.

Figures 17a to 17c show soldering of bond pads of a circuit membrane to a die.

Figure 18 shows bond pads on a die.

Figures 19a, 19b show bonding and de-bonding of a die to a circuit membrane.

Figures 20, 21 show two sides of a circuit membrane.

Figures 22a to 22c show formation of a metal trace in a circuit membrane by a lift-off process.

Figures 23a, 23b show use of a buried etch stop layer to form a circuit membrane having a thinner inner portion.

Figures 24, 25 show a source-integrated light valve 30 for direct write lithography.

Figures 26, 27 are cross-sections of X-ray sources for the device of Figures 24, 25.

Figures 28a to 28b show a coil for the device of Figure 24.

Figures 29a to 29k show portions of a source-external radiation valve for direct write lithography device.

Figures 29l to 29n and 29p show use of fixed freestanding membrane lithography masks.

Figure 30 shows a cross-section of a lithographic 5 tool.

Figures 31a to 31c show cross-sections of a display formed on a membrane.

Figures 32a, 32b show bonding of two circuit membranes.

Figures 32c and 32d show die cut from a circuit membrane and bonded onto a rigid substrate.